

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In Re Application of:)	
Sang Hoo Dong et al.)	
Serial No.: 09/915,437)	Group Art Unit: 2825
Filed: July 26, 2001)	
FOR: METHOD OF LOGIC CIRCUIT)	Examiner: Binh C. Tat
SYNTHESIS AND DESIGN)	
USING A DYNAMIC CIRCUIT)	Confirmation No.: 7370
<u>LIBRARY</u>)	

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PRE-APPEAL BRIEF REQUEST FOR REVIEW

This paper is submitted in response to the Final Office Action mailed June 30, 2006, in the above-identified application, and is filed within the three-month shortened statutory period for response set in the Final Office Action.

Appellants request review of the final rejection in the above-identified application. No amendments are being filed with this request and this request is being filed with a Notice of Appeal. The review is requested for the reasons stated in the following remarks.

1 CLAIMS 1-18 ARE NOT ANTICIPATED BY THE YEE ARTICLE

2 Claims 1-18 stand rejected under 35 U.S.C. §102(b) as being anticipated by “Dynamic
3 Logic Synthesis,” IEEE, 1997, to Yee et al. (“Yee” or the “Yee article”). The Appellants submit
4 that Yee does not anticipate claims 1-18 because Yee does not expressly or inherently disclose all
5 of the limitations required by these claims.

6 The present application includes three independent claims, claims 1, 8, and 13. Due to
7 the nature of the claims, claim 8 will be addressed first in the comments below.

8 Claim 8

9 Independent claim 8 is directed to a method for synthesizing a logic circuit providing a
10 predetermined logical operation, and includes the following limitations:

- 11 (a) defining a logic synthesis block comprising a single dynamic logic circuit; and
12 (b) performing logic synthesis for the predetermined logical operation to produce an
13 intermediate circuit, the logic synthesis utilizing a synthesis library constrained to
14 the single dynamic logic circuit comprising the logic synthesis block.

15 A specific example of logic synthesis performed according to the requirements of claim 8
16 is found starting on page 7, line 6 of the present application. The discussion at page 10, line 15
17 to page 11, line 2 of the Appellants’ response filed April 12, 2006 in this case describes how this
18 specific example in the present application corresponds to the limitations of claim 8.

19 The issue which the Appellants request to be considered in this review with respect to
20 claim 8 is whether Yee teaches performing logic synthesis utilizing a synthesis library
21 constrained to a single dynamic logic circuit as required in element (b) of claim 8.

22 The Final Office Action references Figures 1-8 and pages 345-347 of Yee as disclosing
23 element (b) of claim 8. However, there is no suggestion in the cited portions of Yee for

1 performing logic synthesis utilizing a synthesis library constrained to a single dynamic logic
2 circuit. The only synthesis libraries specifically mentioned in Yee are mentioned at page 347,
3 fourth full paragraph, which clearly describes synthesis libraries having several different types of
4 logic circuits.

5 Because the Yee article does not teach or suggest the limitation set out at element (b) of
6 claim 8, the Appellants submit that claim 8 is not anticipated by Yee and is entitled to allowance
7 along with its respective dependent claims, claims 9-12.

8 Claim 1

9 Claim 1 requires limitations similar to those required by claim 8. However, rather than
10 requiring that logic synthesis is performed utilizing a synthesis library constrained to a single
11 dynamic logic circuit, element (b) of claim 1 requires that logic synthesis is performed with a
12 synthesis library constrained to a particular logic synthesis block, that is, only one logic synthesis
13 block. As discussed above in connection with claim 8, the Yee article discloses only synthesis
14 libraries that include multiple blocks (specifically at least OR, NOR, and NOT gates as indicated
15 at Yee, p. 347, col. 2, second full paragraph). Thus, the Yee article fails to disclose element (b)
16 of claim 1.

17 Element (c) of claim 1 additionally requires producing a final circuit by eliminating
18 unused devices in an intermediate circuit resulting after the logic synthesis constrained to the
19 particular logic synthesis block. However, Yee does not disclose any unused devices after logic
20 synthesis, nor does Yee disclose eliminating unused devices from an intermediate circuit as
21 required by element (c) of claim 1. In contrast to the requirement in claim 1 relating to the
22 removal of unused devices from an intermediate circuit, Yee discloses that after logic synthesis,

1 delay elements are added to the netlist to provide the correct self-timed delays and proper
2 precharge-evaluation clock (See Yee at page 347, Fig. 7 and final paragraph).

3 Because Yee does not disclose at least elements (b) and (c) of claim 1, the Appellants
4 submit that claim 1 is not anticipated by Yee and is entitled to allowance along with its
5 respective dependent claims, claims 2-7.

6 Claim 13

7 Similarly to claim 1, independent claim 13 requires constraining a logic synthesis tool to
8 a particular logic synthesis block, that is, a single logic synthesis block. As discussed above with
9 respect to claim 1, the Yee article does not disclose this limitation. Because Yee does not
10 disclose all of the limitations required by claim 13, the Appellants submit that Yee cannot
11 anticipate claim 13 and that claim 13 is entitled to allowance along with its respective dependent
12 claims, claims 14-18.

13
14 REJECTIONS OVER YEE HAVE BEEN APPLIED INCONSISTENTLY

15 The Appellants note that the rejections in view of the Yee article were originally made in
16 the Office Action mailed March 29, 2005, but omitted in the Office Action mailed July 13, 2005,
17 in favor of rejections over different art. Surprisingly, the claims were again rejected in view of
18 Yee in the Office Action mailed January 13, 2006. The Appellants respectfully submit that the
19 original rejections in view of Yee should have been withdrawn in the July 13, 2005 Office
20 Action, and should not have been reinstated.

1 CONCLUSION

2 For all of the above reasons, the Appellants respectfully request reconsideration and
3 allowance of claims 1-18.

4 Respectfully submitted,

5 The Culbertson Group, P.C.

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8 Dated: 29 Sept 2006

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